



Product/process change notification: **PDP/25/15526**

8 inches Wafer Diameter Conversion for Filter and ESD Protection automotive grade devices at ST Tours (France)

PDP Group
Discrete & Filter Division

Initial issue date: 24-Jul-2025 (Advanced PCN)

Final issue date: 17-Aug-2026 (Final PCN at qualification completion)

Product family	Technology	Package
PROTECTION	ESD and Filter	Various

Description of the change

Following Corporate **PCI 15383 (Early Notification)**, about Company reshaping program, please be informed that Die manufacturing line in 6 inches at ST Tours (France) for Filter and ESD Protection automotive grade devices listed here below will be converted to 8 inches wafer diameter.

Change summary:

	Former	New
Wafer manufacturing location	6" ST Tours (France)	8" ST Tours (France)

Marking and traceability:

Traceability of the change will be ensured by an internal codification (Finished Good/Type) printed on the carton box label.

Commercial part number/Order code	Former Finished Good/Type	New Finished Good/Type
ESDA25LY	AESD25LY/C	Starting by   ESDA25LY\$C

Affected product

EMIF06-1005MX12Y
ESDA14V2LY
ESDA25LY
ESDA25SC6Y
ESDA5V3LY
ESDA5V3SC6Y
ESDA6V1-5SC6Y
ESDA6V1LY

Reason

ST manufacturing reshaping program - Corporate PCI - Early Notification.

Date of implementation

First shipments forecast: Dec-2026

Impact of the change

Form	Not impacted
Fit	Not impacted
Function	Not impacted
Reliability	Not impacted
Processibility	Not impacted

Qualification of the change (plan)

Qualification will be performed according to JESD47 and AECQ-101.

Disposition of former products

Delivery of current products will be done until stock depletion.

Current Finished Good Last Order Date: Apr-2026

Orders received after the expiration of the current Finished Good Last Order Date should be treated as orders for the new, modified Finished Good as outlined in this PCN.

Qualification results

Qualification report including qualification results is enclosed at the end of this document: 26039QRP.

Qualification completion: August-2026

Sampling plan

Qualification samples will be available on demand (through Sales), starting from **Aug-2026**.

For sample(s) request, please inform FSE (Field Sales Engineer) to insert corresponding **Non-Standard Samples Order** (a single Commercial Product for each request) with **PCN reference** as additional information.

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Qualification Report

8 inches Wafer Diameter Conversion for Filter and ESD Protection devices at ST Tours (France)

General Information			Locations	
Product Line	IPAD / Protection		Wafer Fab	ST TOURS - FRANCE
Product Description	ASD - TRANSIL / IPAD LINE FILTER		Assembly Plant	ST SHENZHEN - CHINA ST SUBCONTRACTOR - CHINA ST SUBCONTRACTOR - MALAYSIA
Product Perimeter	EMIF02-1003M6	ESDA6V1SC5	Reliability Lab	ST TOURS – FRANCE
	EMIF03-SIM02M8	ESDA6V1SC6		
	EMIF04-1005M8	ESDA6V1U1RL		
	EMIF06-1005M12	ESDA6V1W5		
	EMIF06-MSD02N16	ESDALC6V1-1M2		
	EMIF06-1005MX12Y	ESDALC6V1-5P6		
	ESDA14V2BP6	ESDALC6V1M3R		
	ESDA14V2L	ESDALC6V1P5		
	ESDA14V2SC6	ESDALC6V1P6		
	ESDA19SC6	ESDALC6V1W5		
	ESDA25-4BP6	SM2T3V3A		
	ESDA25W	SMLVT3V3		
	ESDA5V3L	USBUF01W6		
	ESDA5V3SC5	USBUF02W6		
	ESDA5V3SC6	ESDA6V1-5SC6		
	ESDA6V1-4BC6	ESDA25SC6Y		
	ESDA6V1-5W6	ESDA6V1-5SC6Y		
	ESDA5V3LY	ESDA25LY		
	ESDA5V3SC6Y	ESDA14V2LY		
	ESDA6V1LY			
Product Group	APMS		Reliability Assessment	PASS
Product Division	Discrete & Filter			
Package	QFN-6L, QFN-8L, QFN-12L, QFN-16L SOT666, SOT23-3L, SOT23-5L, SOT23-6L SOT323-3L, SOT323-5L, SOT323-6L SO-8, SOD882, SOT883, SOT-665 SOT-666IP, DO-216AA, SMB			
Maturity level step	QUALIFIED			

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	12-Aug-2026	21	Ilyes TAYEB BEY	Timothée PINGAULT Digitally signed by Timothée PINGAULT Date: 2026.08.12 12:16:14 +02'00'	8 inches Wafer Diameter Conversion for Filter and ESD Protection devices at ST Tours (France)

Note: This report is a summary of the qualification trials performed in good faith by STMicroelectronics in order to evaluate the potential risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101 Rev.E	Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications
AEC-Q005	Pb-Free Test Requirements
AEC-Q006	Qualification Requirements for Components Using Copper (Cu) Wire Interconnections
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices
MIL-STD-750C	Test method for semiconductor devices

2 GLOSSARY

BS	Bond Shear
DPA	Destructive Physical Analysis
DS	Die Shear
ESD	Electro-Static Discharge
EV	External Visual
H3TRB	High Humidity High Temperature Reverse Bias
HTRB	High Temperature Reverse Bias
PC	Preconditioning
PV	Parametric Verification
RSH	Resistance to Soldering Heat
SS	Sample Size
TC	Temperature Cycling
UHASt	Unbiased Highly Accelerated Stress Test
WBS	Wire Bond Strength

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify 8 inches Wafer Diameter Conversion for Filter and ESD Protection automotive grade devices at ST Tours (France), following Corporate PCN 15526 & PCN 15527 about company reshaping program.

Table of involved product:

Commercial Product	Package	Commercial Product	Package
EMIF02-1003M6	QFN-6L	ESDA6V1L	SOT23-3L
EMIF03-SIM02M8	QFN-8L	ESDA6V1SC5	SOT23-5L
EMIF04-1005M8	QFN-8L	ESDA6V1SC6	SOT23-6L
EMIF06-1005M12	QFN-12L	ESDA6V1U1RL	SO-8
EMIF06-MSD02N16	QFN-16L	ESDA6V1W5	SOT323-5L
ESDA14V2BP6	SOT666	ESDALC6V1-1M2	SOD882
ESDA14V2L	SOT23-3L	ESDALC6V1-5P6	SOT666
ESDA19SC6	SOT23-6L	ESDALC6V1M3R	SOT883
ESDA25-4BP6	SOT666	ESDALC6V1P5	SOT-665
ESDA25W	SOT323-3L	ESDALC6V1P6	SOT-666IP
ESDA5V3L	SOT23-3L	ESDALC6V1W5	SOT323-5L
ESDA5V3SC5	SOT23-5L	SM2T3V3A	DO-216AA
ESDA5V3SC6	SOT23-6L	SMLVT3V3	SMB
ESDA6V1-4BC6	SOT23-6L	USBUF01W6	SOT323-6L
ESDA6V1-5SC6	SOT23-6L	USBUF02W6	SOT323-6L
ESDA6V1-5W6	SOT323-6L	ESDA5V3LY	SOT23-3L
ESDA25SC6Y	SOT23-6L	ESDA5V3SC6Y	SOT23-6L
EMIF06-1005MX12Y	QFN-12L	ESDA6V1LY	SOT23-3L
ESDA6V1-5SC6Y	SOT23-6L	ESDA25LY	SOT23-3L
ESDA14V2LY	SOT23-3L		

PCN	Item	Before	After
15526 & 15527	Wafer diameter	6 inches (ST Tours)	8 inches (ST Tours)

The reliability test methodology used follows the JESD47: « Stress Test driven Qualification Methodology » and AEC-Q101 revE guidelines.

The reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- H3TRB, UHAST to check the robustness to corrosion and the good package hermeticity.
- RSH to check compatibility of package with customer assembly.

3.2 **Conclusion**

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

Based on these results, 8 inches wafer diameter conversion for Filter and ESD Protection devices at ST Tours (France) is compliant with AEC-Q101 Rev.E.

4 DEVICE CHARACTERISTICS

4.1 Device description

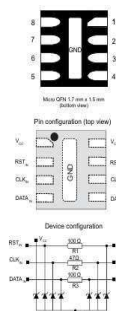
Refer to product datasheets.



EMIF03-SIM02M8

Datasheet

3 line IPAD, EMI filter for SIM card applications



Features

- SIM card EMI low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 1.7 mm x 1.5 mm
- Very thin package: 0.6 mm max.
- High efficiency in ESD suppression on external pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging
- Lead free package
- Easy layout and flexibility thanks to I/O topology
- Low clamping voltage
- Complies with following standards:
 - IEC 61000-4-2 level 4 external pins
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
 - IEC 61000-4-2 level 2 internal pins
 - 2 kV (air discharge)
 - 2 kV (contact discharge)
- MIL STD 883G - Method 3015-7 Class 3A (all pins)

Applications

Where EMI filtering in ESD sensitive equipment is required:

- Keyboard for mobile phones
- Computers and printers
- Communication systems
- MCU boards

Description

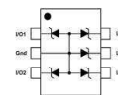
The EMIF03-SIM02M8 is a 3 line highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference. This filter includes ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 15 kV on the external pins.

life.augmented

ESDA6V1-5SC6Y

Datasheet

Automotive 5 lines TVS for ESD protection



Features

- AEC-Q101 qualified
- 5 unidirectional TVS functions
- UL 94, V0
- J-STD-020 MSL level 1
- Benefit:
 - Suitable for high density boards
- Complies with the standard ISO 10605 / IEC 61000-4-2: C = 150 pF, R = 330 Ω
 - ±30 kV (air discharge)
 - ±18 kV (contact discharge)
- Complies with the standard ISO 10605: C = 330 pF, R = 330 Ω
 - ±20 kV (air discharge)
 - ±13 kV (contact discharge)
- Complies with the standard ISO 7637-3
 - Pulse 3a: VS = -150 V
 - Pulse 3b: VS = +100 V

Applications

Where ESD and EOS transient overvoltage protection in susceptible equipment is required, such as:

- Information - entertainment
- Signal communications
- Connectivity
- Comfort and convenience

Description

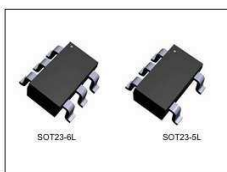
The ESDA6V1-5SC6Y is a monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against ESD. It clamps the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transient.



ESDAxxSCxY

Automotive quad-line Transil™ transient voltage suppressor (TVS) for ESD protection

Datasheet - production data



Features

- 4 unidirectional Transil functions
- 400 W peak pulse power (8/20 μs)

Benefits

- High EOS and ESD protection levels
- Suitable for high density boards
- AEC-Q101 qualified

Complies with the following standards:

- ISO 10605: C = 150 pF, R = 330 Ω
 - 30 kV (air discharge)
 - 30 kV (contact discharge)
- ISO 10605: C = 330 pF, R = 330 Ω
 - 30 kV (air discharge)
 - 30 kV (contact discharge)
- ISO 7637-2
 - Pulse 1: VS = -100 V
 - Pulse 2a: VS = +50 V
 - Pulse 3a: VS = -150 V
 - Pulse 3b: VS = +100 V

Applications

Where ESD and EOS transient overvoltage protection in susceptible equipment is required, such as:

- Information - entertainment
- Signal communications
- Connectivity
- Comfort and convenience

Description

The ESDAxxSCxY devices are monolithic voltage suppressors designed to protect components which are connected to data and transmission lines against ESD.

They clamp the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transient.

Figure 1. Pin configuration

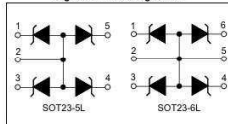


Table 1. Device summary

Order code	V _{BR} (min.)	Package
ESDA5V3SC6Y	5.3	SOT23-6L
ESDA6V1SC6Y	6.1	SOT23-6L
ESDA14V2SC6Y	14.2	SOT23-6L
ESDA14V2SC6Y	14.2	SOT23-6L
ESDA25SC6Y	25	SOT23-6L



ESDAxxSCx

Quad Transil™ array for ESD protection

Datasheet - production data



Description

The ESDAxxSCxY and ESDAxxSC6 are monolithic voltage suppressors designed to protect components which are connected to data and transmission lines against ESD.

They clamp the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transient.

Figure 1. ESDAxxSC5 functional diagram

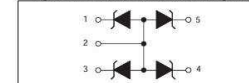


Figure 2. ESDAxxSC6 functional diagram

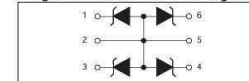


Table 1. Device summary

Order code	V _{BR} min.	Package
ESDA5V3SC5	5.3 V	SOT23-5L
ESDA5V3SC6	5.3 V	SOT23-6L
ESDA6V1SC5	6.1 V	SOT23-5L
ESDA6V1SC6	6.1 V	SOT23-6L
ESDA14V2SC5	14.2 V	SOT23-5L
ESDA14V2SC6	14.2 V	SOT23-6L
ESDA19SC6	19 V	SOT23-6L
ESDA25SC6	25 V	SOT23-6L

Features

- 4 unidirectional ESD protection
- 400 W peak pulse power (8/20 μs)
- Benefits
 - High ESD protection level: up to 30 kV
 - High integration
 - Suitable for high density boards
- Complies with the following standards
 - IEC 61000-4-2 level exceed level 4:
 - 30 kV (air discharge)
 - 30 kV (contact discharge)
- MIL STD 883C - Method 3015-7: class3B
 - human body model

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Other telephone set
- Set top boxes

TM: Transil is a trademark of STMicroelectronics.



Application Specific Discretes A.S.D.

ESDA6V1U1 TRANSIL ARRAY FOR ESD PROTECTION

APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- COMPUTERS
- PRINTERS
- COMMUNICATION SYSTEMS
- GSM HANDSETS AND ACCESSORIES
- CAR RADIO

It is particularly recommended for parallel port protection where the line interface withstands only 2 kV ESD surge.

FEATURES

- 6 UNIDIRECTIONAL TRANSIL FUNCTIONS
- LOW LEAKAGE CURRENT: I_{le} max. < 2 μ A
- 200 W PEAK PULSE POWER (8/20 μ s)

DESCRIPTION

The ESDA6V1U1 is a monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against ESD.

It clamps the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transients.

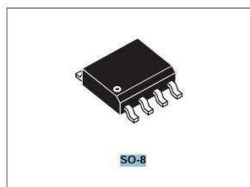
BENEFITS

High ESD protection level : up to 25 kV
High integration
Suitable for high density boards

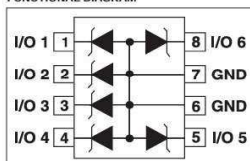
COMPLIES WITH THE FOLLOWING STANDARDS :

IEC61000-4-2 : level 4

MIL STD 883C-Method 3015-6 : class3
(human body model)



FUNCTIONAL DIAGRAM



August 2002 - Ed. 3A

1/8



ESDLC6V1-5P6

ESD protection for high speed interface

Features

- Diode array topology
- Low capacitance (12 pF typical)
- Lead-free package

Benefits

- Low capacitance uni-directional ESD protection.
- Low PCB space consuming, 2.5 mm² max. footprint
- Low leakage current
- High reliability offered by monolithic integration

Complies with the following standards

- IEC 61000-4-2 level 4:
 - 8 kV (contact discharge)
 - 15 kV (air discharge)
- MIL STD 883C-Method 3015-7: class3B
 - Human body model

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

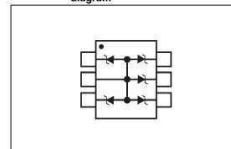
Description

The ESDLC6V1-5P6 is a monolithic array designed to protect up to 5 lines against ESD transients.

The device is ideal for high speed interface applications where both reduced printed circuit board space and power absorption capability are required.



Figure 1. ESDLC6V1-5P6 functional diagram



November 2007

Rev 3

1/8

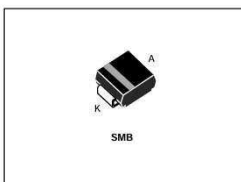
www.st.com



SMLVT3V3

Low voltage Transil™

Datasheet - production data



Description

This is a Transil diode designed specifically to protect sensitive 3.3 V equipment against transient overvoltages.

Transil diodes provide high overvoltage protection by clamping action. Their instantaneous response to transient overvoltages make them particularly suited to protect voltage sensitive devices such as MOS technology and low voltage supplied ICs.

TM: Transil is a trademark of STMicroelectronics

Features

- Peak pulse power 600 W (10/1000 μ s)
- Stand-off voltage 3.3 V
- Unidirectional type
- Low clamping factor
- Fast response time
- JEDEC registered package outline

April 2017

DocID4146 Rev 5

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USBUF

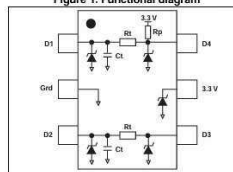
EMI filter and line termination for USB upstream ports

Datasheet - production data



SOT323-6L

Figure 1. Functional diagram



Features

- Monolithic device with recommended line termination for USB upstream ports
- Integrated R_t series termination and C_t bypassing capacitors.
- Integrated ESD protection
- Small package size
- Benefits
 - EMI / RF1 noise suppression
 - Required line termination for USB upstream ports
 - ESD protection exceeding IEC 61000-4-2 level 4
 - High flexibility in the design of high density boards
 - Tailored to meet USB 1.1 standard

- Complies with the following standards IEC 61000-4-2, level 4
 - $\pm$ 15 kV (air discharge)
 - $\pm$ 8 kV (contact discharge)
- MIL STD 883C, Method 3015-7
 - Class 3 C $\approx$ 100 pF; R $\approx$ 1500 Ω
 - 3 positive strikes and 3 negative strikes (F = 1 Hz)

Application

EMI Filter and line termination for USB upstream ports on:

- USB Hubs
- PC peripherals

Description

The USB specification requires upstream ports to be terminated with pull-up resistors from the D+ and D- lines to Vbus. On the implementation of USB systems, the radiated and conducted EMI should be kept within the required levels as stated by the FCC regulations. In addition to the requirements of termination and EMC compatibility, the computing devices are required to be tested for ESD susceptibility.

The USBUF provides the recommended line termination while implementing a low pass filter to limit EMI levels and providing ESD protection which exceeds IEC 61000-4-2 level 4 standard. The device is packaged in a SOT323-6L which is the smallest available lead frame package (50% smaller than the standard SOT23).

Table 1. Device summary

Order codes	Marking
USBUF01W6	UU1
USBUF02W6	UU2

August 2015

DocID7041 Rev 8

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www.st.com



EMIF06-1005MX12Y

Automotive 6-line IPAD™ low capacitance EMI filter and ESD protection in micro QFN package

Datasheet - production data



Features

- AEC-Q101 qualified
- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering: -34 dB at frequencies from 900 MHz to 1.8 GHz
- Very low PCB space consumption: 3 mm x 1.35 mm
- Very thin package: 0.8 mm max
- High efficiency in ESD suppression on input pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging
- Lead-free package

Complies with the following standards

- IEC 61000-4-2 level 4 input and output pins
 - 15 kV (air discharge)
 - 15 kV (contact discharge)
- ISO10605 input and output pins:
 - 11kV (air discharge)
 - 11kV (contact discharge)
- MIL STD 883G - method 3015-7 Class 3B (all pins)

Applications

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for cars
- DSP inputs
- V2V, V2I communication systems
- Digital tuner inputs

Description

This is a highly integrated 6-line device designed to suppress EM/RFI noise in all systems exposed to electromagnetic interference.

This filter includes ESD protection circuitry, which prevents the application from damages when subjected to ESD surges up to 15 kV on the input pins.

Figure 1: Pin configuration (top view)

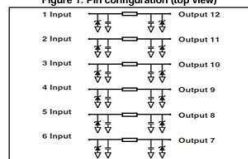
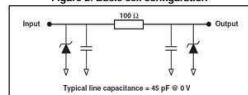


Figure 2: Basic cell configuration



April 2017

DocID030405 Rev 2

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This is information on a product in full production.

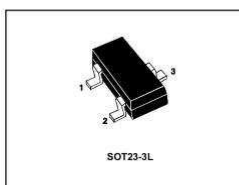
www.st.com



ESDAL

Dual Transil™ array for ESD protection

Datasheet - production data



Features

- Unidirectional device
- Low leakage current (I_{le} max. $< 20 \mu A$ at V_{ias})
- 300 W peak pulse power (8/20 μs)

Benefits

- High ESD protection level: up to 30 kV
- High integration
- Suitable for high density boards

Complies with the following standards

- IEC 61000-4-2 (exceeds level 4):
 - 30 kV (air discharge)
 - 30 kV (contact discharge)

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Entertainment
- Signal communications
- Connectivity
- Comfort and convenience

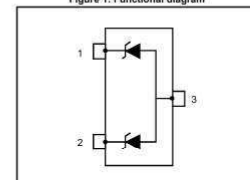
Description

This device is a diode array designed to protect 1 line or 2 lines against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

It can also be used as bidirectional suppressor by connecting only pin 1 and 2.

Figure 1: Functional diagram



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This is information on a product in full production.

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4.2 Construction Note

	ESDA25SC6Y
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	ASD - TRANSIL
Assembly information	
Assembly site	ST SUBCONTRACTOR - MALAYSIA
Package description	SOT23-6L
Molding compound	ECOPACK@2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - MALAYSIA

	EMIF06-1005MX12Y
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	IPAD LINE FILTER
Assembly information	
Assembly site	ST SUBCONTRACTOR - MALAYSIA
Package description	QFN-12L
Molding compound	ECOPACK@2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - MALAYSIA

	ESDA6V1-5SC6Y
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	ASD - TRANSIL
Assembly information	
Assembly site	ST SUBCONTRACTOR - MALAYSIA
Package description	SOT23-6L
Molding compound	ECOPACK@2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - MALAYSIA

	EMIF03-SIM02M8
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	IPAD LINE FILTER
Assembly information	
Assembly site	ST SUBCONTRACTOR - CHINA
Package description	Micro QFN 1.7 mm x 1.5 mm
Molding compound	ECOPACK@2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - CHINA

ESDA19SC6	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	ASD - TRANSIL
Assembly information	
Assembly site	ST SUBCONTRACTOR - CHINA
Package description	SOT23-6L
Molding compound	ECOPACK®2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - CHINA

ESDA6V1U1RL	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	ASD - TRANSIL
Assembly information	
Assembly site	ST SHENZHEN - CHINA
Package description	SO-8
Molding compound	ECOPACK®2 ("Halogen-free")
Final testing information	
Testing location	ST SHENZHEN - CHINA

ESDALC6V1-5P6	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	ASD - TRANSIL
Assembly information	
Assembly site	ST SUBCONTRACTOR - CHINA
Package description	SOT666
Molding compound	ECOPACK®2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - CHINA

SMLVT3V3	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	TRANSIL
Assembly information	
Assembly site	ST SUBCONTRACTOR - CHINA
Package description	SMB
Molding compound	ECOPACK®2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - CHINA

USBUF01W6	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	IPAD LINE FILTER
Assembly information	
Assembly site	ST SUBCONTRACTOR - MALAYSIA
Package description	SOT323-6L
Molding compound	ECOPACK®2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - MALAYSIA

ESDA25L	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	ASD - TRANSIL
Assembly information	
Assembly site	ST SUBCONTRACTOR - CHINA
Package description	SOT23-3L
Molding compound	ECOPACK®2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - CHINA

ESDA5V3SC6Y	
Wafer/Die fab. information	
Wafer fab manufacturing location	ST TOURS - FRANCE
Technology / Process family	ASD - TRANSIL
Assembly information	
Assembly site	ST SUBCONTRACTOR - MALAYSIA
Package description	SOT23-6L
Molding compound	ECOPACK®2 ("Halogen-free")
Final testing information	
Testing location	ST SUBCONTRACTOR - MALAYSIA

5 TESTS PLAN AND RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Wafer fab location	Assy plant Location	Comments
L1	EMIF06-1005MX12Y	QFN-12L	ST TOURS - FRANCE	ST SUBCONTRACTOR - MALAYSIA	1 st qualification lot
L2	ESDA6V1-5SC6Y	SOT23-6L			2 nd qualification lot
L3	ESDA25SC6Y	SOT23-6L			3 rd qualification lot
L4	EMIF03-SIM02M8	QFN-8L		ST SUBCONTRACTOR - CHINA	4 th qualification lot
L5	ESDALC6V1-5P6	SOT666		ST SHENZHEN – CHINA	5 th qualification lot
L6	ESDA6V1U1RL	SO-8		ST SUBCONTRACTOR - MALAYSIA	6 th qualification lot
L7	USBUF01W6	SOT323-6L		ST SUBCONTRACTOR - CHINA	7 th qualification lot
L8	SMLVT3V3	SMB		ST SUBCONTRACTOR - MALAYSIA	8 th qualification lot
L9	ESDA19SC6	SOT23-6L		ST SUBCONTRACTOR - CHINA	9 th qualification lot
L10	ESDA6V1-5SC6Y	SOT23-6L		ST SUBCONTRACTOR - MALAYSIA	10 th qualification lot
L11	ESDA19SC6	SOT23-6L		ST SUBCONTRACTOR - CHINA	11 th qualification lot
L12	ESDA25L	SOT23-3L		ST SUBCONTRACTOR - MALAYSIA	12 th qualification lot
L13	ESDA6V1-5SC6Y	SOT23-6L		ST SUBCONTRACTOR - CHINA	13 th qualification lot
L14	ESDA5V3SC6Y	SOT23-6L		ST SUBCONTRACTOR - MALAYSIA	14 th qualification lot

Detailed results in below chapter will refer to these references.

5.2 Test plan

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	All qualification parts tested per the requirements of the appropriate device specification.			X
Pre-conditioning	PC	J-STD-020 JESD22-A113	All qualification parts tested per the requirements of the appropriate device specification.		As per targeted MSL Not applicable for PTH and WLCSP without coating	
MSL research	MSL	J-STD-020			Not applicable for PTH and WLCSP without coating	
External Visual	EV	JESD22B-101	All qualification parts tested per the requirements of the appropriate device specification.		Done during Assembly → Test & Finish inspection	X
Parametric Verification	PV	User specification	L1, L2, L3 L6, L9, L14	6 * 30		X
High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A	L1, L2, L4 L5, L6, L7 L8, L9, L10 L11, L12, L13	12 * 77		X
AC blocking voltage	ACBV	MIL-STD-750-1 M1040 Test condition A			Required for Thyristor only. Alternative to HTRB	
High Temperature Forward Bias	HTFB	JESD22 A-108			Not required, applicable only to LEDs Alternative to HTRB	
High Temperature Operating Life	HTOL				Covered by HTRB or ACSV	
Steady State Operational	SSOP	MIL-STD-750-1 M1038 Test condition B			Required for Voltage Regulator (Zener) only.	
High Temperature Gate Bias	HTGB	JESD 22A-108			Required for Power MOSFET – IGBT only.	
High Temperature Storage Life	HTSL	JESD22 A-103			Covered by HTRB	
Temperature Humidity Storage	THS	JESD22 A-118			Covered by H3TRB	
Temperature Cycling	TC	JESD22A-104	L2, L3, L5 L8, L12	5 * 77		X
Temperature Cycling Hot Test	TCHT	JESD22A-104			Required for Power MOSFET – IGBT only.	
Temperature Cycling Delamination Test	TCDT	JESD22A-104 J-STD-035			Required for Power MOSFET – IGBT only. Alternative to TCHT	
Wire Bond Integrity	WBI	MIL-STD-750 Method 2037			For dissimilar metal bonding systems only	
Unbiased Highly Accelerated Stress Test	UHAST	JESD22A-118 or A101	L3, L5, L12	3 * 77		X
Autoclave	AC	JESD22A-102			Alternative to UHAST	
Highly Accelerated Stress Test	HAST	JESD22A-110			Covered by H3TRB (same failure mechanisms activation).	
High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	L1, L2, L3 L4, L5, L7 L8, L9, L10 L11, L12, L13	12 * 77		X
High Temperature High Humidity Bias	HTHHB	JED22A-101			Not required, LED only	
Intermittent Operational Life / Thermal Fatigue	IOL	MIL-STD-750 Method 1037			For power devices. Not required for Transient Voltage Suppressor (TVS) parts	
Power and Temperature Cycle	PTC	JED22A-105			For power devices. Not required for Transient Voltage Suppressor (TVS) parts Perform PTC if $\Delta T_j > 100^\circ\text{C}$ cannot be achieved with IOL Alternative to IOL	

Stress	Abrv	Reference	Lot	SS	Comments	Test plan
ESD Characterization	ESD HBM	AEC Q101-001 and 005	L1, L2 L3, L14	242		X
ESD Characterization	ESD CDM	AEC Q101-001 and 005				
Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	L1, L2	3 * 2	After H3TRB and TC	X
Physical Dimension	PD	JESD22B-100				
Terminal Strength	TS	MIL-STD-750 Method 2036			Required for leaded parts only	
Resistance to Solvents	RTS	JESD22B-107			Not applicable for Laser Marking	
Constant Acceleration	CA	MIL-STD-750 Method 2006			Required for hermetic packaged parts only.	
Vibration Variable Frequency	VVF	JESD22B-103			Required for hermetic packaged parts only.	
Mechanical Shock	MS	JESD22 B-104			Required for hermetic packaged parts only.	
Hermeticity	HER	JESD22A-109			Required for hermetic packaged parts only.	
Resistance to Solder Heat	RSH	JESD22 A-111 (SMD) B-106 (PTH)	L2, L12	2 * 30		X
Solderability	SD	J-STD-002 JESD22B102				
Dead Bug Test	DBT	ST Internal specification			Mandatory for SMD package Data collection for PTH package	
Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate			Required in case of process change. Not applicable to protection device as no limit specified in the datasheet	
Wire Bond Strength	WBS	MIL-STD-750 Method 2037	L1, L2, L3 L4, L5, L6 L7, L9, L12	9 * 10		X
Bond Shear	BS	AEC-Q101-003	L1, L2, L3 L4, L5, L6 L7, L9, L12	9 * 10		X
Die Shear	DS	MIL-STD-750 Method 2017	L1, L2, L3 L4, L5, L6 L7, L9, L12	9 * 5		X
Unclamped Inductive Switching	UIS	AEC-Q101-004 section 2			Required for Power MOS and internally clamped IGBTs only	
Dielectric Integrity	DI	AEC-Q101-004 section 3			Required for Power MOSFET – IGBT only.	
Short Circuit Reliability Characterization	SCR	AEC-Q101-006			Required for smart power parts only	
Whisker Growth Evaluation	WG	AEC-Q005 JESD201				
Early Life Failure Rate	ELFR	JESD74			Recommended for new techno development in case of identified failure mechanism	
Functional Test (in rush, di/dt,...)	FT	Internal specification				
Repetitive Surge	RS	Internal specification			Required for protection devices only.	
Low Temperature Storage	LTS	JESD-22 A119: 209			AQG324 test for Modules	
Thermal shock test	TST	JESD22-A104			AQG324 test for Modules	
Power Cycling (seconds)	PCsec	MIL-STD750-1 Method1037			AQG324 test for Modules	
Power Cycling (minutes)	PCmin	MIL-STD750-1 Method1037			AQG324 test for Modules	
Mechanical shock	MS	IEC 600068-2-27			AQG324 test for Modules	
Vibration	V	IEC60068-2-6			AQG324 test for Modules	

5.3 Results summary

Test performed as per AEC-Q101-Rev E guidelines.

Test	P C	Std ref.	Conditions	Steps / Duration	SS	Failure/SS												
						L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13
Pre- and Post-Electrical Test		ST datasheet	Vbr, Ir, Vf parameters following product datasheet	-	-	0/2524												
External Visual		JESD22 B-101	All qualification parts submitted for testing passed External & Visual inspection during manufacturing process															
Parametric Verification		ST datasheet	Over part temperature range (note 1)		180	Refer to paragraph 6.1 in Annexes												
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=175°C VR=100% VRRM	1Khrs	77								0/77					
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=150°C VR=100% VRRM	1Khrs	616	0/77	0/77					0/77		0/77	0/77	0/77	0/77	
HTRB	N	MIL-STD-750-1 M1038 Method A	Tj=125°C VR=100% VRRM	1Khrs	231				0/77	0/77	0/77							
TC	Y	JESD22 A-104	-55/+150°C 2cy/h	1Kcy	231		0/77	0/77								0/77		
TC	Y	JESD22 A-104	-65/+150°C 2cy/h	500cy	154					0/77			0/77					
UHASt	Y	JESD22 A-118	130°C; 85% RH 2.3bar	96hrs	231			0/77		0/77						0/77		
H3TRB	Y	JESD22 A-101	85°C; 85% RH VR=100% VRRM	1Khrs	924	0/77	0/77	0/77	0/77	0/77		0/77	0/77	0/77	0/77	0/77	0/77	
ESD		AEC-Q101-001	HBM	-	242	Refer to paragraph 6.2 in Annexes												
DPA		AEC-Q101-004	After TC 1Kcy	-	2		0/2											
			After H3TRB 1Khrs	-	4	0/2	0/2											
RSH	N	JESD22 A-111	85%RH / 85°C 168hrs Dipping 260°C-10s	-	60		0/30									0/30		
WBS		MIL-STD-750 Method 2037	10 bond minimum	-	90	0/10	0/10	0/10	0/10	0/10	0/10	0/10		0/10		0/10		
BS		AEC-Q101-003	10 bond minimum	-	90	0/10	0/10	0/10	0/10	0/10	0/10	0/10		0/10		0/10		
DS		MIL-STD-750 Method 2017	-	-	45	0/5	0/5	0/5	0/5	0/5	0/5	0/5		0/5			0/5	

Note 1: These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet. Parameters distributions are not considered as a ST guarantee under any circumstances.

Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers."

6 ANNEXES

6.1 Parametric verification

➤ ESDA25SC6Y

Characterization ESDA25SC6Y					
Date: 04/06/2026					
Ref: 24683A					
Lab: ST Tours Characterization Lab					
TEST	VBR	IR	αT	VF	VCL
EQUIPEMENT	TSA_491	TSA_491	TSA_491	TSA_491	TSA_491
Condition 1	25°C	25°C	25°C	25°C	25°C
Condition 2	I _r = 1mA	VR=24V	I _r = 1mA	I _f = 10mA	I _{pp} = 9A
Condition 3	On Pin 1	On Pin 1	On Pin 1	On Pin 1	On Pin 1
Min. Datasheet	25				
Typ. Datasheet					
Max. Datasheet	30	1	10	1.2	51
UNIT	V	μA	10-4/°C	V	V
N	30	30	30	30	5
Min.	27.13	0.002	8.25	0.88	40.06
Max.	27.76	0.002	8.55	0.90	40.85
Avg.	27.49	0.002	8.42	0.89	40.51

These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet.
Parameters distributions are not considered as a ST guarantee under any circumstances.

Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

➤ ESDA5V3SC6Y

Characterization ESDA5V3SC6Y					
Date: 31/03/2026					
Ref: 24690A					
Lab: ST Tours Characterization Lab					
TEST	VBR	IR	αT	VF	VCL
EQUIPEMENT	TSA_491	TSA_491	TSA_491	TSA_491	TSA_491
Condition 1	25°C	25°C	25°C	25°C	25°C
Condition 2	I _r = 1mA	VR=3V	I _r = 1mA	I _f = 200mA	I _{pp} = 22A
Condition 3	On Pin 1	On Pin 1	On Pin 1	On Pin 1	On Pin 1
Min. Datasheet	5.3				
Typ. Datasheet					
Max. Datasheet	5.9	2	5	1.25	21
UNIT	V	μA	10-4/°C	V	V
N	30	30	30	30	5
Min.	5.50	0.313	2.25	0.99	12.24
Max.	5.65	0.143	2.65	1.02	12.52
Avg.	5.56	0.472	2.51	1.01	12.38

These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet.
Parameters distributions are not considered as a ST guarantee under any circumstances.

Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

➤ **EMIF06-1005MX12Y**

Characterization EMIF06-1005MX12Y					
Date: 05/05/2026					
Ref: 24691A					
Lab: ST Tours Characterization Lab					
TEST	VBR	IRM	VF	RI/O	Cline
EQUIPEMENT	TSA_491	TSA_491	TSA_491	TSA_491	TSA_491
Condition 1	25°C	25°C	25°C	25°C	25°C
Condition 2	Ir = 1mA	VRM=3V	If = 10mA	Ir = 20mA	Vosc =30mV f=1MHz
Condition 3					
Condition 4	On Pin 1	On Pin 1	On Pin 1	On I/O1 & I/O12	On Pin 1/GND
Min. Datasheet	6		0.5	90	38
Typ. Datasheet	8		1	100	45
Max. Datasheet	10	200	1.5	110	52
UNIT	V	nA	V	V	pF
N	30	30	30	30	6
Min.	7.29	4.22	0.85	96.83	40.58
Max.	7.42	5.28	0.86	98.78	41.28
Avg.	7.36	4.77	0.85	97.84	40.88

These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet.
Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

➤ **ESDA6V1-5SC6Y**

Characterization ESDA6V1-5SC6Y					
Date: 23/06/2026					
Ref: 24804A					
Lab: ST Tours Characterization Lab					
TEST	VBR	IR	αT	VF	VCL
EQUIPEMENT	TSA_491	TSA_491	TSA_491	TSA_491	TSA_491
Condition 1	25°C	25°C	25°C	25°C	25°C
Condition 2	Ir = 1mA	VR=5.2V	Ir = 1mA	If = 200mA	Ipp = 7A
Condition 3	On Pin 1	On Pin 1	On Pin 1	On Pin 1	On Pin 1
Min. Datasheet	6.1				
Typ. Datasheet					
Max. Datasheet	7.2	1	6	1.25	11.4
UNIT	V	μA	10-4/°C	V	V
N	30	30	30	30	5
Min.	6.69	0.036	4.55	1.00	10.77
Max.	6.77	0.204	4.79	1.01	10.92
Avg.	6.72	0.059	4.67	1.00	10.85

These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet.
Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

➤ **ESDA6V1U1RL**

Characterization ESDA6V1U1RL				
Date: 14/04/2026				
Ref: 24684A				
Lab: ST Tours Characterization Lab				
TEST	VBR	IRM	αT	VF
EQUIPEMENT	TSA_491	TSA_491	TSA_491	TSA_491
Condition 1	25°C	25°C	25°C	25°C
Condition 2	Ir = 1mA	VRM=5V	Ir = 1mA	If = 200mA
Condition 3	On Pin 1	On Pin 1	On Pin 1	On Pin 1
Min. Datasheet	6.1			
Typ. Datasheet				
Max. Datasheet	7.2	2	6	1.5
UNIT	V	μA	10-4/°C	V
N	30	30	30	30
Min.	6.71	0.009	3.99	0.93
Max.	6.96	0.305	4.56	0.93
Avg.	6.86	0.047	4.31	0.93

These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet.
Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

➤ **ESDA19SC6**

Characterization ESDA19SC6					
Date: 05/05/2026					
Ref: 24805A					
Lab: ST Tours Characterization Lab					
TEST	VBR	IRM	VCL	αT	VF
EQUIPEMENT	TSA_491	TSA_491	TSA_491	TSA_491	TSA_491
Condition 1	25°C	25°C	25°C	25°C	25°C
Condition 2	Ir = 1mA	VRM=15V	IPP=13A	Ir = 1mA	If = 10mA
Condition 3	On Pin 1	On Pin 1	On Pin 1	On Pin 1	On Pin 1
Min. Datasheet	19				
Typ. Datasheet					
Max. Datasheet	21	0.1	39	8.5	1.2
UNIT	V	μA	V	10-4/°C	V
N	30	30	5	30	30
Min.	19.38	0.002	30.03	7.61	0.81
Max.	19.73	0.003	30.52	8.00	0.83
Avg.	19.54	0.002	30.29	7.77	0.82

These data are indicative values given as information only. Please note that the ST guarantee is the compliance of the products to the ST datasheet.
Parameters distributions are not considered as a ST guarantee under any circumstances.
Please note that these electrical parameters are 100% tested at 25°C at Final stage of back-end manufacturing before deliveries to customers.

6.2 **ESD**

➤ **ESDA25SC6Y**

TEST	ISO 10605 CONTACT
EQUIPEMENT	ESS_S3011A
Condition 1	25°C
Condition 2	C = 330 pF
Condition 3	R = 330 Ω
UNIT	kV
N	30
Min.	> 30
Max.	> 30

➤ **ESDA5V3SC6Y**

TEST	ISO 10605 CONTACT
EQUIPEMENT	ESS_S3011A
Condition 1	25°C
Condition 2	C = 330 pF
Condition 3	R = 330 Ω
UNIT	kV
N	20
Min.	> 30
Max.	> 30

➤ EMIF06-1005MX12Y

TEST	ISO IEC61000 CONTACT	ISO 10605 CONTACT
EQUIPEMENT	ESS_S3011A	ESS_S3011A
Condition 1	25°C	25°C
Condition 2	C = 150 pF	C = 330 pF
Condition 3	R = 330 Ω	R = 330 Ω
UNIT	kV	kV
N	36	36
Min.	> 15	> 11
Max.	> 15	> 11

➤ ESDA6V1-5SC6Y

TEST	IEC61000-4-2 CONTACT	IEC61000-4-2 AIR	ISO 10605 CONTACT	ISO 10605 AIR
EQUIPEMENT	ESS_S3011A	ESD_NX30	ESS_S3011A	ESD_NX30
Condition 1	25°C	25°C	25°C	25°C
Condition 2	C = 150 pF	C = 150 pF	C = 330 pF	C = 330 pF
Condition 3	R = 330 Ω	R = 330 Ω	R = 330 Ω	R = 330 Ω
UNIT	kV	kV	kV	kV
N	30	30	30	30
Min.	> 18	> 30	> 13	> 20
Max.	> 18	> 30	> 13	> 20

6.3 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - Low power dissipation - Max. supply voltage compatible with diffusion process and internal circuitry limitations. Forward: device is forward biased with a current fixed and adjusted to reach the targeted junction temperature	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects. To assess active area and contacts integrity
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop-corn" effect and delamination.
DPA Destructive Physical Analysis	Specific construction analysis on random parts that have successfully completed THB or TC.	To investigate on reliability stresses impact on delamination, corrosion and product construction integrity.
H3TRB High Humidity High Temperature Reverse Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHASt Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
RSH Resistance to Solder Heat	Package is dipped by the leads in a solder bath after initial wet ageing (for SMDs only). Assessment by electrical test + no external crack	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
WBS Wire Bond Strength	To apply the specified stress to the bond, lead wire, or terminal.	To measure bond strength, evaluate bond strength distributions, or to determine compliance with specified bond strength requirements of the applicable acquisition document. This test may be applied to the wire-to-die bond, wire-to-substrate bond, or the wire-to-package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermo-compression, ultrasonic, or related techniques

Test name	Description	Purpose
BS Bond Shear	This test establishes a procedure for determining the strength of the interface between a gold ball bond and a die bonding surface, or an aluminum wedge/stitch bond and a die or package bonding surface, on either pre-encapsulation or post-encapsulation components. This strength measurement is extremely important in determining two features: 1) the integrity of the metallurgical bond which has been formed. 2) the reliability of gold and aluminum wire bonds to die or package bonding surfaces. This test method can be used only when the ball height and diameter for ball bonds, or the wire height (1.25 mil and larger at the compressed bond area) for wedge/stitch bonds, are large enough and adjacent interfering structures are far enough away to allow suitable placement and clearance (e.g., above the bonding	To check the integrity of the metallurgical bond.
DS Die Shear	A sufficient force to shear the die from its mounting shall be applied to the die.	To establish the integrity of the semiconductor die attachment to the package header or other substrate.